Differential LVPECL Voltage Controlled Crystal Oscillator

CRYSTEK CRYSTALS — A DIVISION OF CRYSTEK CORPORATION

CVPD-920 Model
9×14 mm SMD, 3.3V, LVPECL

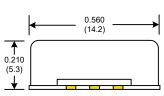|	
Frequency Range:	50 MHz to 125 MHz
Frequency Pulling:	±20ppm APR Min
Temperature Range:	0°C to 70°C
(Option X)	-40°C to 85°C
Storage:	-45°C to 90°C
Input Voltage:	3.3V ±0.3V
Control Voltage:	1.65V ±1.65V
Input Current:	88mA Max
Output:	Differential LVPECL
Symmetry:	45/55% Max @ zero crossing point
Rise/Fall Time:	1ns Max (20% to 80%)
Linearity:	±10% Max
Logic:	Terminated to Vcc-2V into 50 ohms
	"0" = Vcc-1.85V Min, Vcc-1.62V Max
	"1" = Vcc-1.02V Min, Vcc-0.81V Max
Disable Time:	200ns
Start-up Time:	1ms Typical, 2ms Max
Phase Jitter: 12kHz to 80MHz	0.5ps Typical, 1ps RMS Max
Phase Noise: 10Hz	-65 dBc/Hz Typical
100Hz	-98 dBc/Hz Typical
1kHz	-125 dBc/Hz Typical
10kHz	-140 dBc/Hz Typical
100kHz	-145 dBc/Hz Typical
Aging:	<3ppm 1st year, <1ppm every year thereafter

RoHS Compliant

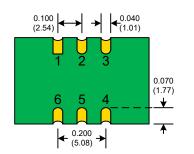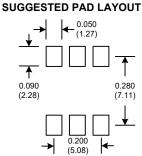**CRYSTEK CORPORATION** — MADE IN THE USA

Designed to meet today's requirements for 3.3V Differential LVPECL applications. The CVPD-920 is produced using our cost saving FR5 PCB and UM-1 overtone crystal technology. This design offers considerable cost savings over other HFF VCXO products when broad frequency pulling is not required. Also available in 14 pin dip fully hermetic package.

Package dimensions: 0.560 (14.2), 0.360 (9.14), 0.210 (5.3)

CRYSTEK P/N / Frequency / Date Code

Pad dimensions: 0.100 (2.54), 0.040 (1.01), 0.070 (1.77), 0.200 (5.08)

SUGGESTED PAD LAYOUT

Pad layout dimensions: 0.050 (1.27), 0.090 (2.28), 0.280 (7.11), 0.200 (5.08)

PAD FINISH: Immersion Gold (ENIG); 5 micro inches maximum

Crystek Part Number Guide

CVPD-920 X - 100.000
#1 #2 #3 #4

#1 Crystek 9×14 SMD PECL VCXO
#2 Model 920
#3 Temp. Range: Blank = 0/70°C, X = -40/85°C
#4 Frequency in MHz: 3 or 6 decimal places

Example:
CVPD-920X-100.000 = 3.3V, 45/55, -40/85°C, 100.000 MHz

Enable/Disable Function

Pin 2	Output Pin
Open	Active
"0" level Vcc-1.620V Max	Active
"1" level Vcc-1.025V Min	Disabled
Disabled State: Pin 4 will assume a fixed level of logic "0" Pin 5 will assume a fixed level of logic "1"	

RECOMMENDED REFLOW SOLDERING PROFILE
900034 (See App Note listed on website)

NOT RECOMMENDED FOR NEW DESIGNS
PLEASE USE CVPD-922 FAMILY

PIN	Function
1	Control Volt
2	E/D
3	GND
4	OUT
5	$\overline{COUT}$
6	Vcc

Rev: L
Date: 14-Sep-2017
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Specifications subject to change without notice.