

RHF7050A

The RHF7050A employs patented analogue temperature compensation to deliver tight stability down to ± 0.28 ppm for high frequency differential outputs up to 1 GHz (or CMOS outputs up to 180 MHz) in a small 7.0 x 5.0 mm hermetically sealed SMD package.

Features

- CMOS, LVPECL, or LVDS output options
- Custom frequency up to 1 GHz output
- Frequency slope and perturbation specifications can be customized
- VCO tilt compensation

Applications

- Networking
- Base Stations
- Communications
- DSL/ADSL
- IP Timing

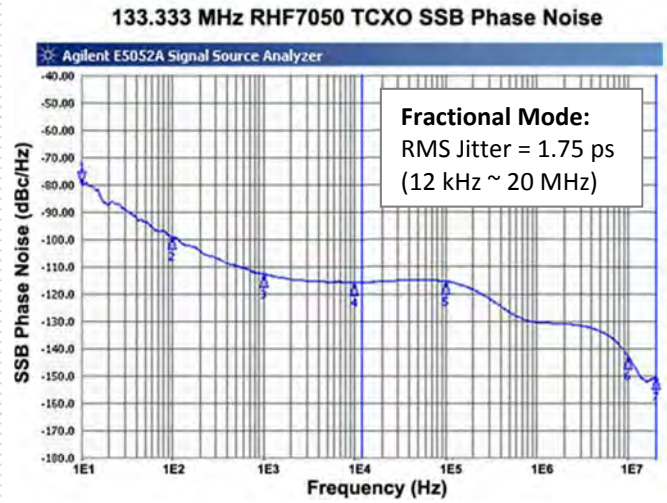
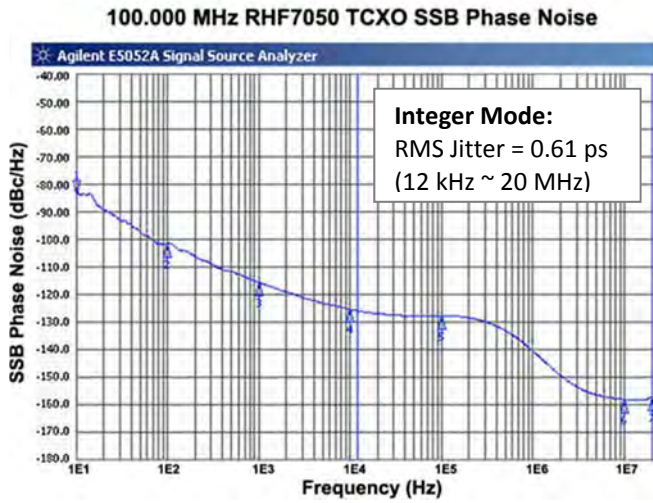
7.0 x 5.0 x 1.65 mm



Standard Specifications

Parameter	Min.	Typ.	Max.	Unit	Test Condition / Description
Nominal frequency		25 – 1000		MHz	CMOS output frequency up to 180MHz
Frequency calibration			± 1	ppm	Initial accuracy at $25 \pm 1^\circ\text{C}$
Reflow shift			± 1	ppm	Pre to post reflow ΔF (measured ≥ 60 minutes after reflow)
Operating temperature range	-40		85	$^\circ\text{C}$	
Frequency stability over temperature			$\pm 0.28 - \pm 2.5$	ppm	Reference to $(F_{\text{max}} + F_{\text{min}})/2$. The best available stability depends on the nominal frequency and selected operating temperature range
Frequency slope			0.1	ppm/ $^\circ\text{C}$	Minimum of 1 frequency reading every 2°C , over the operating temperature range
Supply voltage stability			± 0.1	ppm	•
Load sensitivity			± 10	ppb	• HCMOS, ACMOS: $\pm 5\text{pF}$ variation, • Clipped sine wave / Sine wave: $\pm 10\%$ variation reference to frequency at nominal load
Long term stability (ageing)			± 1 ± 2 ± 6	ppm ppm ppm	Per 1 year Per 2 year Per 10 year
Supply voltage, V_{CC}		3.3		V	$\pm 5\%$
Current (CMOS)			35	mA	25 – 180MHz
Current (LVPECL)			50	mA	25MHz – 1GHz
Current (LVDS)			40	mA	25MHz – 1GHz
Control voltage, V_{C}		1.65		V	
Frequency tuning	± 3			ppm	Nominal control voltage ± 1 V
VCO pin input impedance			100	k Ω	
Frequency tuning linearity			10	%	Deviation from straight line curve fit
Oscillator output (CMOS)					
V_{OL}			$10\%V_{\text{DD}}$	V	15pF capacity load
V_{OH}	$90\%V_{\text{DD}}$			V	15pF capacity load
Duty cycle	48		52	%	Measured at 50% V_{DD} trigger level
Oscillator output (LVPECL)					
V_{OL}			$V_{\text{DD}} - 1.6$	V	50 Ω nominal load
V_{OH}	$V_{\text{DD}} - 1.03$			V	50 Ω nominal load
Duty cycle					Measured at $V_{\text{DD}} - 2\text{V}$
Oscillator output (LVDS)		350		mV	
Duty cycle	48		52		Measured at 1.25V

SSB Phase Noise (Typical value at 25°C)



The standard frequencies as the multiples of 25 (25, 50, 100, 125, etc.)

Please send an email to Sales@rakon.com for availability of other frequencies.

Model Outline and Recommended Pad Layout

1 TOP VIEW

FRONT VIEW

BOTTOM VIEW

RECOMMENDED PAD LAYOUT - TOP VIEW

PIN CONNECTIONS

1*	V _C , NC
2*	E/D
3	GND
4	NC
5	Output
6*	Complementary Output (LVPECL/LVDS), NC
7	V _{DD}
8	NC

* Depending on the specifications

NOTE: Outline unit is mm.