



## Features

- Very low phase jitter
- Ceramic package and metal lid assures extreme accuracy and high reliability.
- Lead-free soldering is available.
- Applications: Networking systems, Test and measurement, Servers and storage systems, Profession video equipments, FPGA/ASIC clock generation

## Specifications

Item	Symbol	Specifications			
		Min.	Typ.	Max.	Note
Frequency	F0	10MHz		400 MHz	As specified
Frequency Stability	FT			±50 ppm	See ※1 below
Storage temperature range		-55°C		+125°C	
Operating temperature range	TR	-20°C		+70°C	Commercial(standard)
		-40°C		+85°C	Industrial(standard)
Supply voltage	Vcc	3.135V	3.30V	3.465V	or 2.5V±5%
Current consumption	Icc/OE			60mA	
Disable current	Icc/OD			20mA	
Logic type	LT	PECL			
Output voltage "0"level	VoL			Vcc-1.55V	
Output voltage "1"level	VoH	Vcc-1.2V			
Output load		See Test Circuit			
Symmetry	SYM	45%		55%	Mesured 50%Vcc
Rise time / Fall time	TR/TF			350ps	Mesured 20/80% of waveform
Phase jitter	RMS(1-σ)		0.8ps		(Offset frequency:12kHz to 20MHz)

※1 Stability includes all combinations of operating temperature ,load changes , rated input (supply) voltage changes,initial calibration tolerance(25°C),aging(5 years at 40°C average effective ambient temperature),shock and vibration.

### Output Enable /Disable Function

Item	Min.	Typ.	Max.	Note
Input Voltage(OE pin),Output Enable	0.7Vcc			or open
Input Voltage(OE pin),Output Disable			0.3Vcc	Outputs disabled to Hi-Z
Output Disabel Delay			200ns	
Output Enabel Delay			200ns	
Start up time			10ms	

- Bypass capacitor should be connected between V<sub>DD</sub> and GND due to the stabilized operation for the crystal oscillator.
- Please consult us for customized specifications.
- All specifications and markings subjected to change without notice.

