

# Model 655

## Ultra Low Jitter LVPECL or LVDS Clock

### Features

- Ceramic Surface Mount Package
- Ultra Low Phase Jitter Performance, 100fs Typical
- Fundamental or 3<sup>rd</sup> Overtone Crystal Design
- Frequency Range 80 – 170MHz \*
- +2.5V or +3.3V Operation
- Output Enable Standard
- Tape and Reel Packaging, EIA-418



Part Dimensions:  
5.0 × 3.2 × 1.2mm • 62.00mg

### Applications

- SerDes
- Storage Area Networking
- Broadband Access
- SONET/SDH/DWDM
- PON
- Ethernet/GbE/SyncE
- Fiber Channel
- Test and Measurement

Standard Frequencies, 100fs Maximum

- 125.00MHz	- 156.25MHz
- 155.52MHz	- 161.1328MHz

\* Check with factory for availability.

### Description

CTS Model 655 is a low cost, high performance clock oscillator supporting differential LVPECL or LVDS outputs. Employing the latest IC technology, M655 has excellent stability and very low jitter/phase noise performance.

### Ordering Information

Model	Output Type	Frequency Code [MHz]	Frequency Stability	Temperature Range	Supply Voltage	Packaging																															
655	P	XXX or XXXX	3	I	3	T																															
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Notes:

- 1] Refer to document 016-1454-0, Frequency Code Tables. 3-digits for frequencies <100MHz, 4-digits for frequencies 100MHz or greater.
- 2] Consult factory for availability of 6I Stability/Temperature combination.

**Not all performance combinations and frequencies may be available.**  
**Contact your local CTS Representative or CTS Customer Service for availability.**

## Electrical Specifications

### Operating Conditions

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Maximum Supply Voltage	$V_{CC}$	-	-0.5	-	5.0	V
Supply Voltage	$V_{CC}$	$\pm 5\%$	2.375 3.135	2.5 3.3	2.625 3.465	V
Supply Current						
LVPECL	$I_{CC}$	Maximum Load	-	55	88	mA
LVDS			-	45	66	
Operating Temperature	$T_A$	-	-20 -40	+25	+70 +85	$^{\circ}\text{C}$
Storage Temperature	$T_{STG}$	-	-40	-	+125	$^{\circ}\text{C}$

### Frequency Stability

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Range						
LVPECL	$f_0$	-		80 - 170		MHz
LVDS				80 - 170		
Frequency Stability [Note 1]	$\Delta f/f_0$	-		20, 25, 50 or 100		$\pm\text{ppm}$
Aging	$\Delta f/f_{25}$	First Year @ +25 $^{\circ}\text{C}$ , nominal $V_{CC}$	-3	-	3	ppm

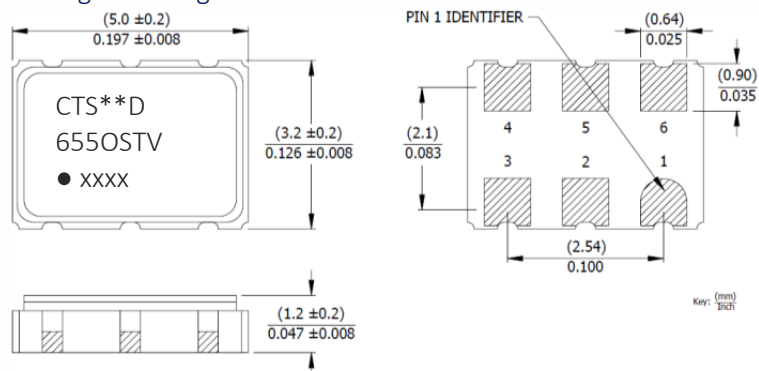
1.] Inclusive of initial tolerance at time of shipment, changes in supply voltage, load, temperature and 1st year aging.

### Output Parameters

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Output Type	-	-		LVPECL		-
Output Load	$R_L$	Terminated to $V_{CC} - 2.0\text{V}$	-	50	-	Ohms
Output Voltage Levels						
	$V_{OH}$	PECL Load, -20 $^{\circ}\text{C}$ to +70 $^{\circ}\text{C}$	$V_{CC} - 1.025$	-	$V_{CC} - 0.880$	V
	$V_{OL}$		$V_{CC} - 1.810$	-	$V_{CC} - 1.620$	
	$V_{OH}$	PECL Load, -40 $^{\circ}\text{C}$ to +85 $^{\circ}\text{C}$	$V_{CC} - 1.085$	-	$V_{CC} - 0.880$	V
	$V_{OL}$		$V_{CC} - 1.830$	-	$V_{CC} - 1.555$	
Output Duty Cycle	SYM	@ $V_{CC} - 1.3\text{V}$	45	-	55	%
Rise and Fall Time	$T_R, T_F$	@ 20%/80% Levels, $R_L = 50\text{ Ohms}$	-	0.3	0.7	ns
Output Type	-	-		LVDS		-
Output Load	$R_L$	Between Outputs	-	100	-	Ohms
Output Voltage Levels						
	$V_{OH}$	LVDS Load	-	1.43	1.60	V
	$V_{OL}$		0.90	1.10	-	
Output Duty Cycle	SYM	@ 1.25V	45	-	55	%
Differential Output Voltage	$V_{OD}$	$R_L = 100\text{ Ohms}$	247	330	454	mV
Offset Voltage	$V_{OS}$	LVDS Load	1.125	1.25	1.375	V
Rise and Fall Time	$T_R, T_F$	@ 20%/80% Levels, $R_L = 100\text{ Ohms}$	-	0.4	0.7	ns

### Mechanical Specifications

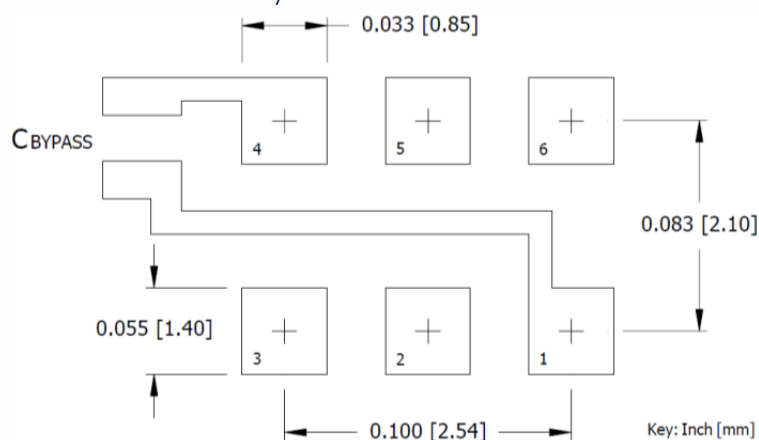
#### Package Drawing



#### Marking Information

- \*\* - Manufacturing Site Code.
- D - Date Code. See Table I for codes.
- O - Output Type; P or E = LVPECL, L or V = LVDS. [Refer to Ordering Information]
- V - Voltage Code; 3 = 3.3V, 2 = 2.5V.
- xxxx - Frequency Code.  
3-digits, frequencies below 100MHz  
4-digits, frequencies 100MHz or greater  
[See document 016-1454-0, Frequency Code Tables.]

#### Recommended Pad Layout



#### Notes

- JEDEC termination code (e4). Barrier-plating is nickel [Ni] with gold [Au] flash plate.
- Reflow conditions per JEDEC J-STD-020; +260°C maximum, 20 seconds.
- MSL = 1.

#### Pin Assignments

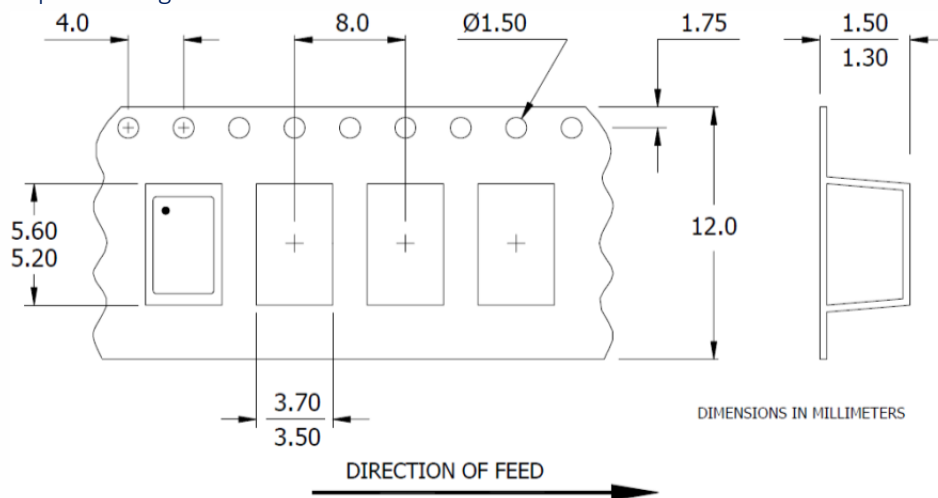
Pin	Symbol	Function
1	EOH or N.C.	Enable [std] or No Connect
2	N.C. or EOH	No Connect or Enable [opt]
3	GND	Circuit & Package Ground
4	Output	RF Output
5	Output	Complimentary RF Output
6	V <sub>CC</sub>	Supply Voltage

Table I - Date Code

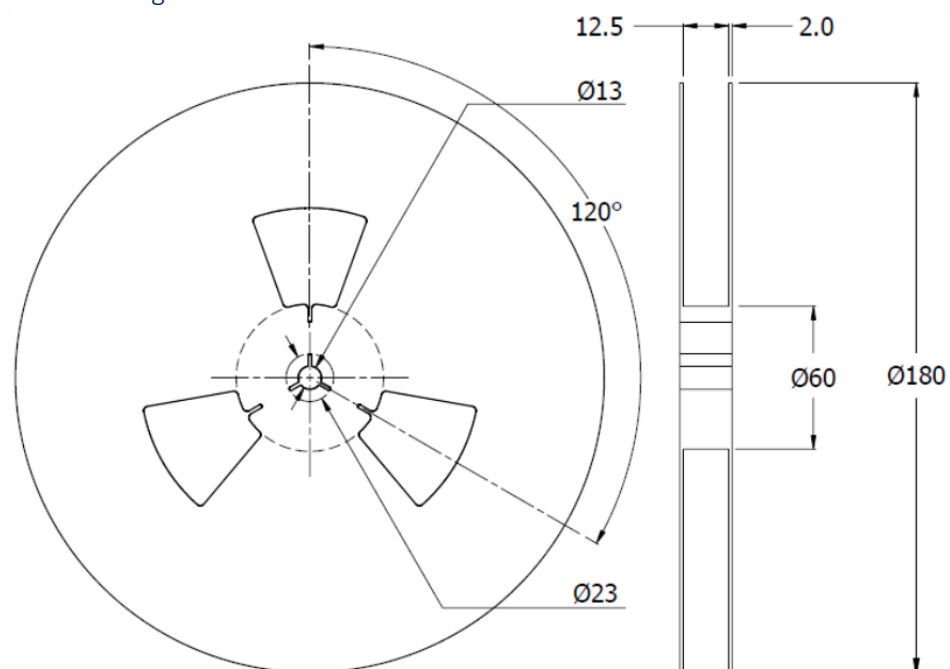
YEAR		MONTH														
		JAN	FEB	MAR	APR	MAY	JUN	JUL	AUG	SEP	OCT	NOV	DEC			
2001	2005	2009	2013	2017	A	B	C	D	E	F	G	H	J	K	L	M
2002	2006	2010	2014	2018	N	P	Q	R	S	T	U	V	W	X	Y	Z
2003	2007	2011	2015	2019	a	b	c	d	e	f	g	h	j	k	l	m
2004	2008	2012	2016	2020	n	p	q	r	s	t	u	v	w	x	y	z

## Packaging - Tape and Reel

### Tape Drawing



### Reel Drawing



### Notes

1. Device quantity is 1k pieces per 180mm reel.
2. Complete CTS part number, frequency value and date code information must appear on reel and carton labels.